CLAIMS:

1. A semiconductor integrated circuit comprising:

a plurality of circuit blocks each having a clock distribution line pattern;

a first signal path for transmitting a data signal from said first circuit block to a second circuit block; and

at least a first buffer circuit connected to said first signal path in such a manner as to constitute said first signal path and at least a second buffer circuit connected to said second signal path in such a manner as to constitute said second signal path;

wherein said circuit blocks, said first and second signal paths, and said first and second buffer circuits are formed on a single semiconductor substrate;

wherein said clock signal and said data signal are transmitted in parallel to each other on said first and second signal paths, and said data signal is taken by said second circuit block by said clock signal; and

wherein said first and second signal paths have substantially the same wiring conductor length.

2. A semiconductor integrated circuit according to Claim 1, wherein said first circuit block has an output latch circuit for latching the data signal to be transmitted, said second circuit block has an input

latch circuit for latching the data signal to be received, and said output latch circuit and said input latch circuit are configured to perform the latch operation in response to the clock signals before and after, respectively, being transmitted from said first circuit block to said second circuit block.

3. A semiconductor integrated circuit according to Claim 2, wherein said first circuit block is configured to send the next data signal and the clock signal to said first and second signal paths before arrival of the transmitted data signal clock signal at said second circuit block.

4. A semiconductor integrated circuit according to Claim 1, wherein said second circuit block includes a plurality of circuits operated in synchronism with the internal clock generated based on the clock signal received from said second signal path, and said clock distribution line pattern of said second circuit block is configured to distribute said internal clock to said plurality of circuits through the substantially same length of path.

5. A semiconductor integrated circuit according to Claim 4, wherein said circuit blocks are configured in such a manner that when said data signal is not sent out to said second circuit block from said first circuit block, said clock signal is not sent out from said first circuit block to said second circuit block.

6. A semiconductor integrated circuit according to Claim 1, wherein a third signal path for feeding back the clock signal received by said second circuit block to said first circuit block is inserted between said first and second circuit blocks, and said first circuit block includes a phase adjusting circuit for adjusting the phase of the clock signal sent out from said first circuit block in such a manner that the clock signal in said first circuit block is in phase with the clock signal fed back.

7. A semiconductor integrated circuit according to Claim 6, wherein said phase adjusting circuit includes a phase detecting circuit for generating a phase difference signal representing the phase difference obtained by comparing the phase of the clock signal in said first circuit block with the phase of said clock signal fed back, and variable delay circuits with the delay time thereof variable based on the phase difference signal from said phase detecting circuit.

8. A semiconductor integrated circuit according to Claim 1, wherein said second circuit block includes a plurality of circuits operated in synchronism with a clock signal different from said clock signal received, and the clock distribution line pattern of said second circuit block is configured to distribute said different clock signal to said plurality of the circuits through paths having substantially the same length.

9. A semiconductor integrated circuit according to Claim 8, wherein said second circuit block includes means for taking the serial data signal received from said first signal path, based on the received clock signal and storing said serial data signal for at least two periods of said received clock signal, and means for reading the data signal stored in said storage means by a clock signal different from said received clock signal.

10. A semiconductor integrated circuit according to Claim 9,

wherein said second circuit block includes a phase shifting circuit for generating a clock signal out of phase by one half period of the data transmission cycle based on the received clock, and a phase adjusting circuit for generating a clock signal giving a timing of taking data to said holding means based on the clock signal generated by said phase shifting circuit, and

wherein said phase adjusting circuit operates to adjust the phase of the clock signal supplied to said holding means in such a manner that the clock signal generated by said phase-shifting circuit is in phase with the phase of the clock signal supplied to said holding means.

11. A semiconductor integrated circuit according to Claim 10, wherein said holding means is configured

to take said received data signal substantially at the center between the changing points of said received data signal.